Main Memory (Part I)

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Motivation and Background

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- These instructions may cause additional loading from and storing to specific memory addresses.

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- Cache sits between main memory and registers.

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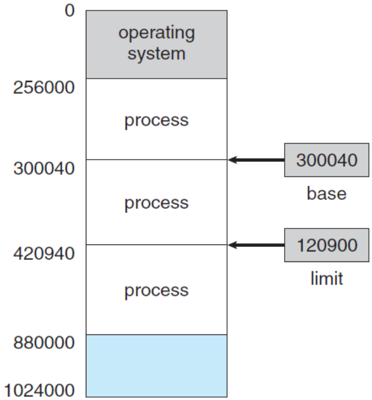
- This protection is provided by the hardware.
- A separate memory space for each process.
  - Determining the range of legal addresses that the process may access.

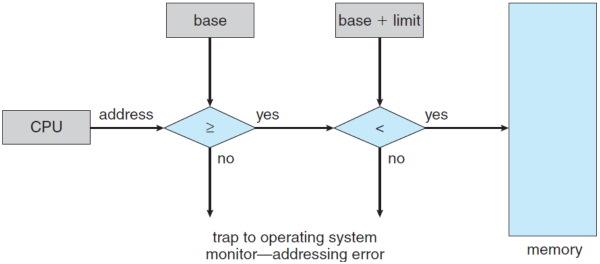
Base and Limit Registers

- A pair of base and limit registers define the logical address space.
- CPU must check every memory access generated in user mode to be sure it is between base and limit for that user.



Hardware Address Protection

- Any attempt by a user program to access OS memory or other users' memory results in a trap to the OS, which treats the attempt as a fatal error.



Address Binding

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- A user process can reside in any part of the physical memory.
  - Without support, must be loaded into address 00000.

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  - Linker or loader will bind relocatable addresses to absolute addresses, e.g., 74014.

Binding of Instructions and Data to Memory (1/3)

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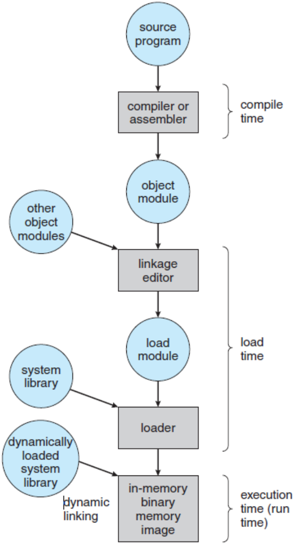

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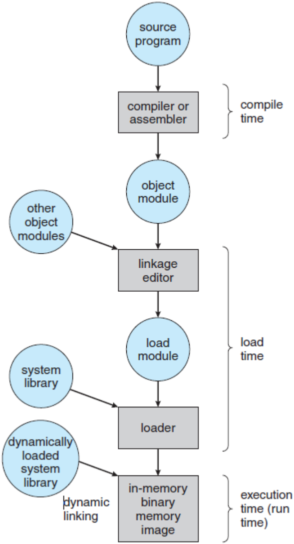
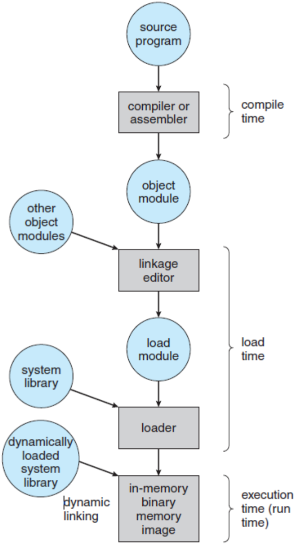
- Compile time: if memory location known a priori, absolute code can be generated.
  - Must recompile code if starting location changes.



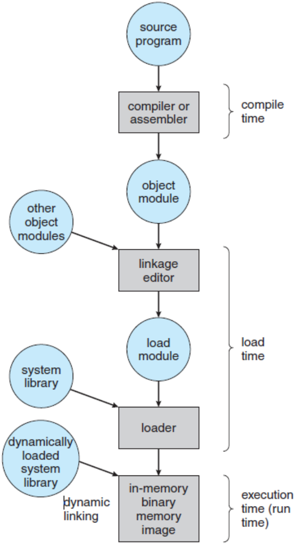
Binding of Instructions and Data to Memory (2/3)

- Load time: must generate relocatable code if memory location is not known at compile time.
  - Final binding is delayed until load time.
  - If the starting address changes, we need only reload the user code to incorporate this changed value.



Binding of Instructions and Data to Memory (3/3)

- Execution time: binding delayed until run time if the process can be moved during its execution from one memory segment to another.
  - Need hardware support



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- The concept of a logical address space that is bound to a separate physical address space is central to proper memory management.

Logical vs. Physical Address Space (2/2)

- Logical and physical addresses are the same in compile-time and load-time address-binding schemes.

- Logical and physical addresses differ in execution-time address-binding scheme.

Memory-Management Unit (MMU) (1/2)

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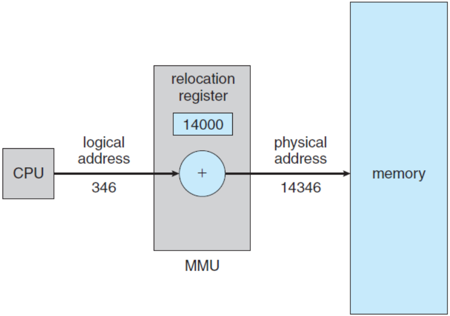
- As a simple scheme, the value in the relocation register is added to every address generated by a user process at the time it is sent to memory.
  - Base register now called relocation register.



Memory-Management Unit (MMU) (2/2)

- Two different types of addresses:
  - Logical addresses: range 0 to max
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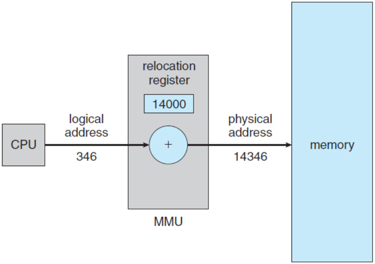

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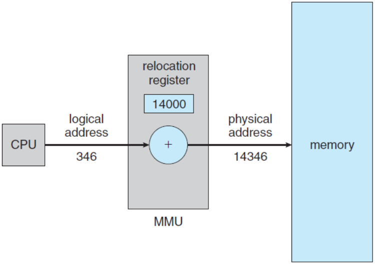

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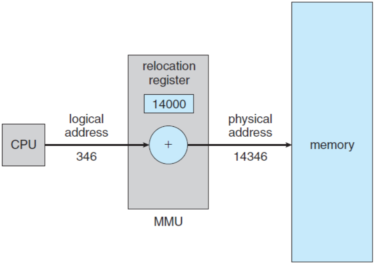
- These logical addresses must be mapped to physical addresses before they are used.



Dynamic Linking and Loading

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- All routines kept on disk in relocatable load format.

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- OS can help by providing libraries to implement dynamic loading.

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- Static linking: system libraries and program code combined by the loader into the binary program image.
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- Stub: small piece of code, used to locate the appropriate memory-resident library routine.
- Stub replaces itself with the address of the routine, and executes the routine.

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- Dynamic linking is particularly useful for shared libraries.

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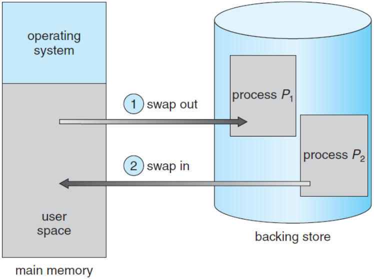

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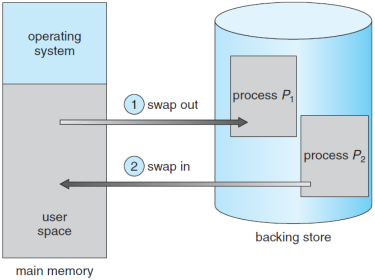
- Total memory space of processes can exceed physical memory.



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- Pending I/O: cannot swap out as I/O would occur to wrong process.
  - Or always transfer I/O to kernel space, then to I/O device.
  - Known as double buffering, adds overhead.

Swapping (3/3)

- Standard swapping not used in modern OSs, but modified version is common.
- Swap only when free memory extremely low.
- Disabled again once memory demand reduced below threshold.

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- Example:
  - 100MB process swapping to hard disk with transfer rate of 50MB/sec.
  - Swap out time of 2s + swap in of same sized process.
  - Total context switch swapping component time of 4s.

Swapping on Mobile Systems (1/2)

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- Flash memory based
  - Small amount of space
  - Limited number of write cycles
  - Poor throughput between flash memory and CPU on mobile platform

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- Android terminates apps if low free memory, but first writes application state to flash for fast restart.

Contiguous Memory Allocation

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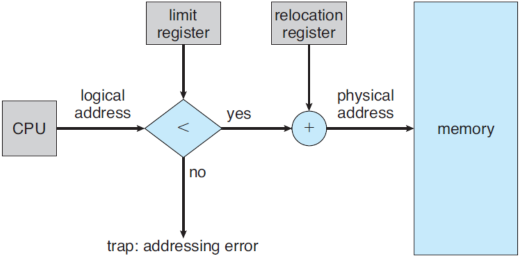
- Main memory usually into two partitions:
  - Resident OS, usually held in low memory with interrupt vector.
  - User processes then held in high memory.
  - Each process contained in single contiguous section of memory.

Contiguous Allocation (2/2)

- Relocation registers used to protect user processes from each other, and from changing OS code and data.
  - Base register contains value of smallest physical address.
  - Limit register contains range of logical addresses.
  - MMU maps logical address dynamically.



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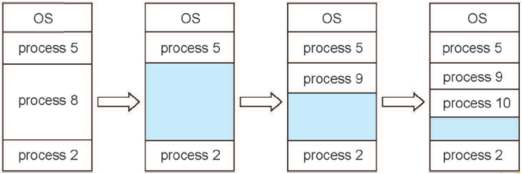

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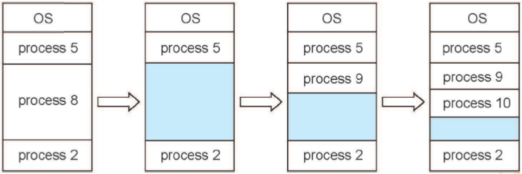

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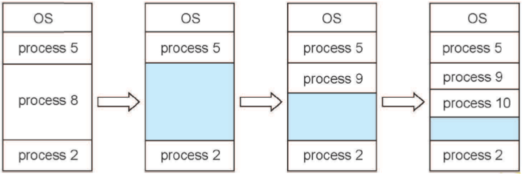

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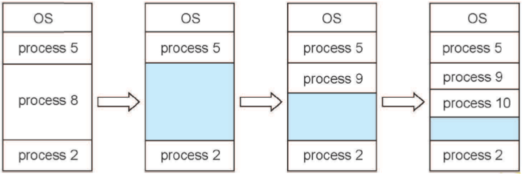

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- OS maintains information about: allocated partitions and free partitions (hole)

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- First-fit and best-fit better than worst-fit in terms of speed and storage utilization.

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- First fit analysis reveals that given N blocks allocated, $0.5N$ blocks lost to fragmentation: 50-percent rule

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- Compaction is possible only if relocation is dynamic, and is done at execution time.
- I/O problem
  - Latch job in memory while it is involved in I/O
  - Do I/O only into OS buffers.

Fragmentation (3/3)

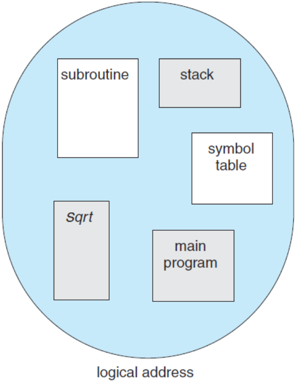
- Another possible solution to the external fragmentation problem: permit the logical address space of the processes to be noncontiguous.

- Two techniques:
  - Segmentation
  - Paging

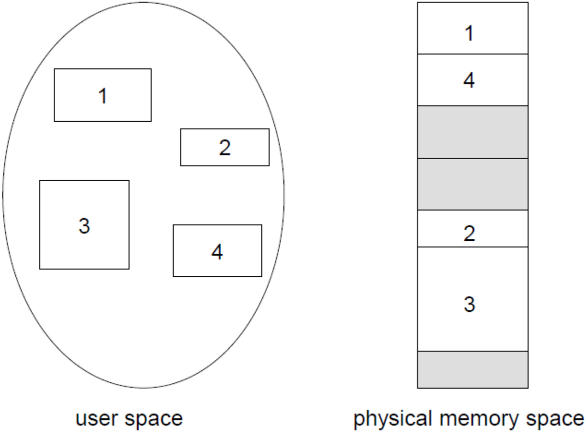
Segmentation

Fragmentation (2/2)

- Memory-management scheme that supports user view of memory.
- A program is a collection of segments.
- A segment is a logical unit such as:
  - Main program
  - Procedure
  - Function
  - Object
  - ...



Logical View of Segmentation



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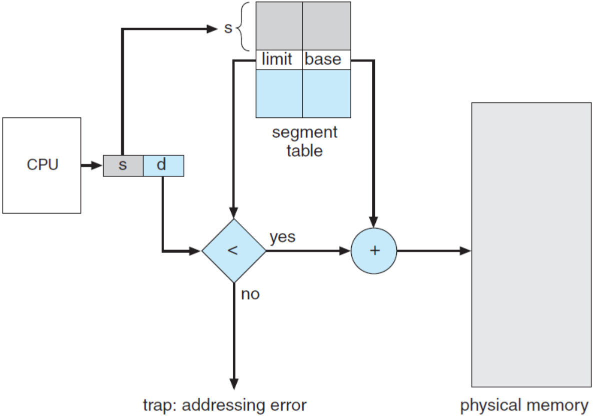
- Segment table: maps two-dimensional user-defined addresses into one-dimensional physical address.
- Each table entry has:
  - Base: contains the starting physical address where the segments reside in memory
  - Limit: specifies the length of the segment

Segmentation Hardware



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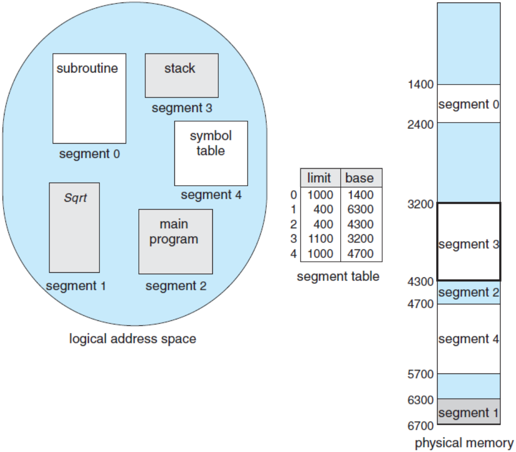

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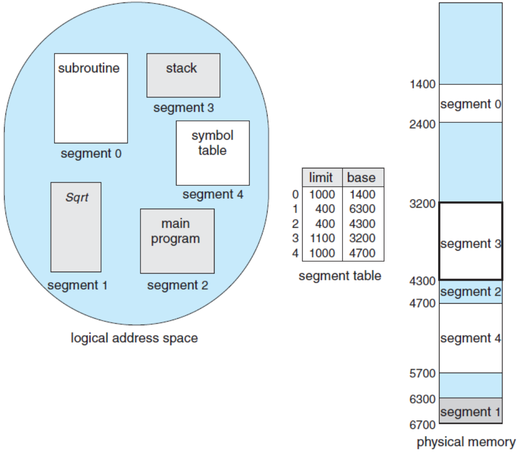
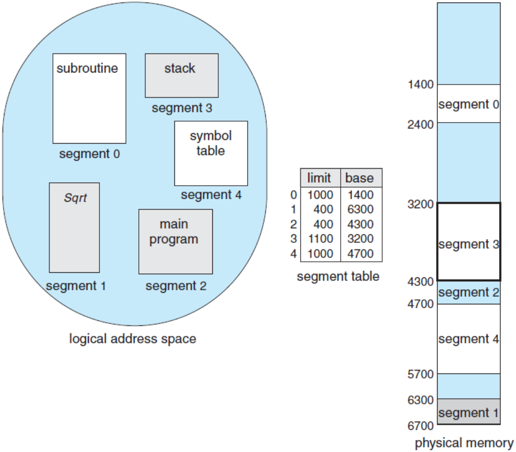


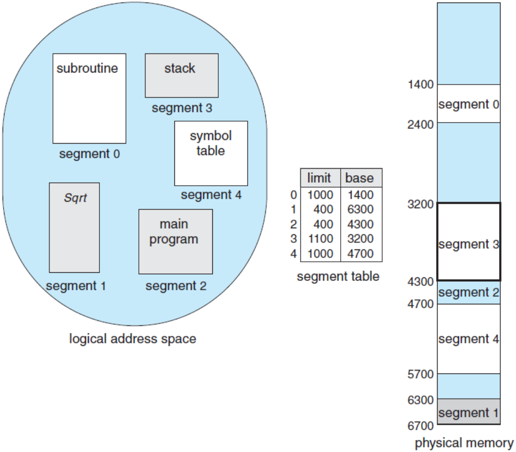
- A reference to byte 53 of segment 2: $4300 + 53 = 4353$

Segmentation Example



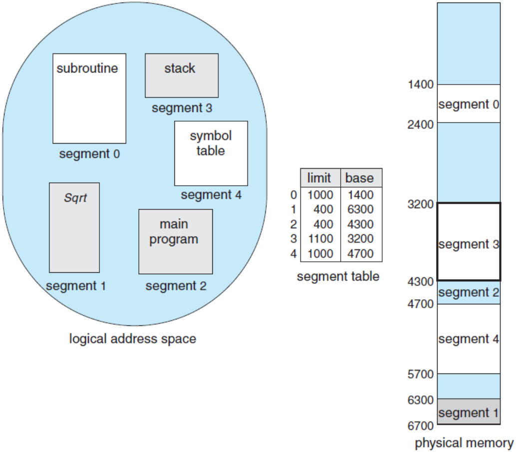
- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3:

Segmentation Example



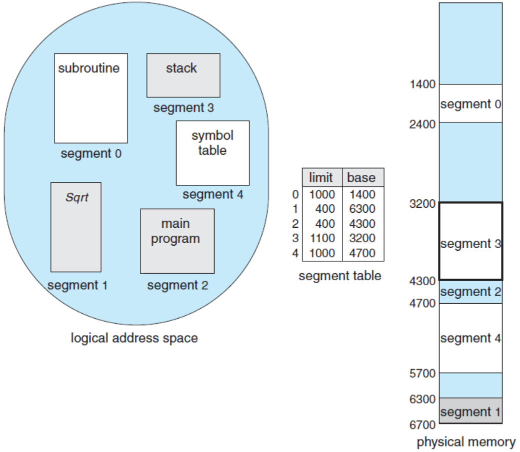
- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3: $3200 + 852 = 4052$

Segmentation Example



- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3: $3200 + 852 = 4052$
- A reference to byte 1222 of segment 0:

Segmentation Example



- A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- A reference to byte 852 of segment 3: $3200 + 852 = 4052$
- A reference to byte 1222 of segment 0: trap to OS

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- External and internal fragmentation: compaction, segmentation, paging
- Segmentation: noncontiguous address, user view of memory

Questions?

Acknowledgements

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